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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kresge *et al.*

Examiner: Nguyen, Donghai D.

Serial No.: 10/040,745

Art Unit: 3729

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For: **METHOD OF MAKING AN ELECTRONIC PACKAGE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF OF APPELLANTS

This Appeal Brief, pursuant to the Notice of Appeal filed July 23, 2003, is an appeal from the rejection of the Examiner dated April 23, 2003.

REAL PARTY IN INTEREST

International Business Machines, Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 80-97 are currently pending.

STATUS OF AMENDMENTS

There are no After-Final Amendments which have not been entered.

SUMMARY OF INVENTION

The present invention discloses a method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections. The semiconductor chip may have a first surface including a plurality of contact sites thereon. Provided is a thermally conductive layer including first and second opposing surfaces. First and second dielectric layers are positioned on the first and second opposing surfaces of the thermally conductive layer, respectively. See specification, page 6, lines 5-20. First and second pluralities of electrically conductive members are positioned on the first and second dielectric layers, respectively. Each of the first and second pluralities of said electrically conductive members are adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively. See specification, page 7, line 25 - page 8, line 4; page 12, lines 16-20. The thermally conductive layer is comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of the solder connections between the first plurality of electrically conductive members and the semiconductor chip and between the second plurality of electrically conductive members and the circuitized substrate. See specification, page 8, lines 12-14.

The positioning of the first and second dielectric layers on the first and second opposing surfaces of said thermally conductive layer, respectively, may comprise laminating the first and second dielectric layers onto the first and second opposing surfaces at a pressure of from about

1000 to about 1500 psi and at a temperature of from about 600 to about 750 °F. See specification, page 13, lines 5-10.

The positioning of the first and second pluralities of electrically conductive members on the first and second dielectric layers, respectively, may comprise: laminating a first copper foil and a second copper foil respectively onto the first and second dielectric layers; and etching selected portions of said first and second copper foils to respectively produce first and second pluralities of the electrically conductive members. See specification, page 13, line 19 - page 14, line 17.

The method may further include the steps of: positioning a third dielectric layer on the first dielectric layer and on the first plurality of electrically conductive members; removing portions of the third dielectric layer to expose portions of the first plurality of electrically conductive members; and forming a first plurality of openings (i.e., microvias) within the third dielectric layer to expose at least a portion of at least one of the first plurality of electrically conductive members. Removing portions of the third dielectric layer may be performed by laser ablating. Each opening may include an internal wall and exposing a portion of at least one of the first plurality of electrically conductive members. A conductive layer may be plated on the internal wall and on the exposed portion of at least one of the first plurality of electrically conductive members to define a plurality of microvias. A first solder paste may be applied onto the conductive layer. The solder paste may be reflowed to form a first plurality of solder connections on the first plurality of electrically conductive member. See specification, page 14, line 18 - page 15, line 12.

The method may further include the steps of: positioning a fourth dielectric layer on said

second dielectric layer and on said second plurality of electrically conductive members; removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members. Removing portions of the fourth dielectric layer may be performed by laser ablating. See specification, page 14, line 18 - page 15, line 9.

The semiconductor chip may have a first surface including a plurality of contact sites thereon. See specification, page 6, lines 6-8. Respective ones of the first plurality of solder connections may be connected to respective ones of the plurality of contact sites on the semiconductor chip. See specification, page 8, lines 1-4.

The method may further include providing a first plurality of solder connections on the first plurality of electrically conductive members, which may be performed by: forming a plurality of openings in said third dielectric layer, each of said openings including an internal wall and exposing a portion of at least one of said first plurality of electrically conductive members; plating a conductive layer on said internal wall of said plurality of openings and on said exposed portion of said at least one of said first plurality of electrically conductive members to define a plurality of microvias; applying a first solder paste onto said conductive layer; and reflowing said solder paste to form a first plurality of solder connections on the first plurality of electrically conductive members. Connecting respective ones of the first plurality of solder connections to respective ones of the plurality of contact members on the semiconductor chip may include the steps of: applying a second solder paste onto said respective ones of the first plurality of solder connections; positioning the respective ones of the contact members of the

semiconductor chip against the respective ones of the first plurality of solder connections; and reflowing the second solder paste and the respective ones of the first plurality of solder connections to electrically connect the semiconductor chip to the multi-layered interconnect structure. See specification, page 14, line 18 - page 15, line 9; page 8, lines 1-11.

The circuitized substrate may have a first surface including a plurality of contact pads thereon. A second plurality of solder connections may be provided on the second plurality of conductive members of the multi-layered interconnect structure. Respective ones of the second plurality of said solder connections may be connected to respective ones of the plurality of contact pads on the circuitized substrate to make electrical connections therebetween. See specification, page 12, lines 16-20.

A first electrically conductive layer may be positioned within the first dielectric layer. A second electrically conductive layer may be positioned between the first electrically conductive layer and the thermally conductive layer. The second electrically conductive layer may comprise a first plurality of shielded signal conductors. See specification, page 7, lines 12-24.

ISSUES

1. Whether claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b) are unpatentable over US Patent 4,882,454 to Peterson et al.

2. Whether claims 81, 88, and 92 under 35 U.S.C. §103(a) are unpatentable over Peterson et al.

3. Whether claims 89 and 90 under 35 U.S.C. §103(a) are unpatentable over Peterson et al. in view of US Patent 5,691,041 to Frankeny et al.

GROUPING OF CLAIMS

The claims are grouped as shown in Table 1.

Table 1

Group	Issue	Claims	Do Claims of Group Stand or Fall Together?
1	1	80, 82-86, 87	Yes
2	1	91, 93-97	Yes
3	2	81, 88, 92	No
4	3	89, 90	No

The claims of Group 2 do not stand and fall together with the claims of Group 1, because the claims of Group 2 include the following issues not present in any of the claims of Group 1: whether Peterson teaches the feature: "positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors"

The claims of Group 3 do not stand and fall together with the claims of Groups 1-2, because the claims of Group 3 have been rejected under 35 U.S.C. §103(a) whereas the claims of Groups 1-2 have been rejected under 35 U.S.C. §102(b).

The claims of Group 4 do not stand and fall together with the claims of Groups 1-3,

because the claims of group 4 were rejected under 35 U.S.C. §103(a) over Peterson in view of Frankeny, whereas the claims of Groups 1-2 have been rejected under 35 U.S.C. §102(b), and whereas the claims of group 3 were rejected under 35 U.S.C. §103(a) over Peterson.

The claims of Group 3 do not stand and fall together because: claim 81 was rejected under 35 U.S.C. §102(b), claim 88 was rejected under 35 U.S.C. §103(a) over Peterson, and claim 92 was rejected under 35 U.S.C. §103(a) over Peterson in view of Frankeny

The claims of Group 4 do not stand and fall together because claim 90 includes the following issue not present in claim 89: whether Peterson in view of Frankeny teaches or suggests the feature: "connecting respective ones of said second plurality of said solder connections to respective ones of said plurality of contact pads on said circuitized substrate to make electrical connections therebetween"

ARGUMENT

Issue 1

CLAIMS 80, 82-87, 91, AND 93-97 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §102(b) OVER US PATENT 4,882,454 TO PETERSON ET AL.

The Examiner rejected claims 1 claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b) as allegedly being unpatentable over US Patent 4,882,454 to Peterson et al.

Claim 80

The Examiner alleges: "Regarding claim 80, Peterson et al. disclose a method of making a multi-layer interconnect structure, the method comprising: providing a thermally conductive layer (102); positioning first (310) and second (311) dielectric layers on the thermally conductive layer; and position first (312) and second (313) pluralities of electrically conductive members on the first and second dielectric layers, each of said first and second pluralities of electrically conductive members adapted for having solder connection (103 and 104) thereon, and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53)."

Appellants respectfully contend that Peterson does not anticipate claim 80, because Peterson does not teach each and every feature of claim 80.

A first example of why Peterson does not teach each and every feature of claim 80, Peterson does not teach the following feature of claim 80: "positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members

adapted for having solder connections **thereon** for being electrically connected to a semiconductor chip and a circuitized substrate" (emphasis added). The word "thereon" refers to the first and second pluralities of said electrically conductive members.

The Examiner argues that Peterson teaches that electrically conductive members 312 and 313 of FIG. 4 of Peterson are adapted for having alleged solder connections 103 and 104 thereon. In response, Appellants point out that solder connection 103 and 104 are not shown on FIG. 4 of Peterson as alleged by the Examiner, but are shown on FIG. 1 of Peterson. A comparison of FIGS. 1 and 4 of Peterson makes it clear that Peterson does not teach the preceding feature of claim 80 as will be explained next.

In FIG. 1 the electrically conductive members 105 corresponding to electrically conductive members 312 and 313 of FIG. 4 are internal to the substrate of FIG. 1 and are separated by one dielectric layer 101 from thermally conductive layer 102 of FIG. 1 and are separated from the alleged solder connections 103 and 104 by two dielectric layers 101, in order to have geometrical consistency between the electrically conductive members 312 and 313 of FIG. 4 as cited by the Examiner and the corresponding electrically conductive members 105 of FIG. 1. Thus the alleged solder connections 103 and 104 of FIG. 1 are not **on**, and are significantly separated from, the electrically conductive members 312 and 313 of FIG. 4 in violation of claim 80, so that claim 80 is not anticipated by Peterson.

A second example of why Peterson does not teach each and every feature of claim 80, Peterson does not teach the following feature of claim 80 "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to

substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate".

The Examiner alleges that Peterson teaches "the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53)".

In response to the preceding argument by the Examiner, Appellants cite Peterson as stating in col. 2, lines 44- 49 that "[i]deal performance in a surface mount application is achieved when CTE, thermal, weight and electrical properties are optimized by proper choice of materials and geometries. Core modifications can also be made to enhance thermal, CTE or weight properties when specific needs must be met. These involve the use of clad materials in the core, or composite cores of graphite, polymer, and copper." **The preceding disclosure in Peterson is non-specific** and therefore does not disclose specific features of claim 80. While Peterson discloses that optimization could be achieved by "proper choice of materials and geometries", Peterson does not state what is to be optimized and what choice of geometries could be utilized to achieve optimization.

For example, Peterson does not specifically disclose optimization "**to substantially prevent failure of said solder connections** between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate" (emphasis added) as required by claim 80.

As another example, Peterson does not specifically disclose "said thermally conductive layer being comprised of a material having a **selected thickness** and coefficient of thermal

expansion to substantially prevent failure ..." (emphasis added) as required by claim 80. Thus, Peterson teaches selection of geometry without any disclosure of a selection of thickness. Appellants maintain that selection of geometry does not inherently imply a selection of thickness since geometry includes many attributes (thickness, linear dimensions other than thickness, areas, volumes, etc.).

Additionally, col. 2, lines 44-47 of Peterson does not specifically or inherently identify the thermally conductive layer 102 as a layer whose geometry is to be controlled, and there are several structural portions (e.g., layers other than layer 102) in FIG. 1 of Peterson whose geometry may be controlled in accordance with col. 2, lines 44-47 of Peterson. Appellants note that claim 80 specifically recites a thickness condition on the thermally conductive layer.

Appellants further maintain that col. 1, lines 40-43 of Peterson recites "[i]t is therefore an object of the invention to have a printed wiring board structure that possesses similar thermal expansion characteristics to surface mount components to be attached", which does not state anything about "substantially preventing failure of said solder connections."

Appellants note that col. 2, lines 13-19 of Peterson teaches "The elongated pads (103 and 104) along with the underlying vias (106 and 107) allow a spring action to be used to help absorb any difference in thermal expansion between the printed wiring board and the surface mount device. This greatly reduces the stress that is placed on the soldered connection and thus promotes reliability." Thus, the reduction in stress on the solder connection is due to "the elongated pads (103 and 104) along with the underlying vias (106 and 107)" and not due to the thermally conductive layer as required by claim 80.

Appellants respectfully contend that in order to support a rejection of a claim under 35

U.S.C. §102(b) through use of a reference, the Examiner must demonstrate that every feature of the claim is either expressly or inherently taught by the reference. Appellants respectfully contend that in order prove that a reference inherently teaches a feature, it is not sufficient to argue that the feature may be present. The Examiner must present an argument (e.g., a logical argument, an argument based on application of a physical law, etc.) that the feature **must** be present, which the Examiner has not done for the claims rejected under 35 U.S.C. §102(b). Instead, the Examiner has relied on conjecture and speculation.

A third example of why Peterson does not teach each and every feature of claim 87, Peterson does not teach the following feature of claim 87: "each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a **semiconductor chip** and a circuitized substrate" (emphasis added). Appellants contend that Peterson does not teach a semiconductor chip and does not teach solder connections adapted to be connected to a semiconductor chip. In addition, since the Examiner has not addressed this feature of claim 80, Applicants contend that the Examiner has not satisfied the Examiner's burden of proof in relation to claim 80.

Based on the preceding arguments, Appellants respectfully maintain that Peterson does not anticipate claim 80, and the claim 80 is in condition for allowance.

Claims 82-86

Since claims 82-86 depend from claim 80, which Appellants have argued *supra* to be patentable under 35 U.S.C. §102(b), Appellants maintain that claims 82-86 are patentable under 35 U.S.C. §102(b).

Claim 87

Appellants respectfully contend that Peterson et al. does not anticipate claim 87, because Peterson does not teach each and every feature of claim 87.

A first example of why Peterson does not teach each and every feature of claim 87, Peterson does not teach the following feature of claim 87: "providing a first plurality of solder connections on said first plurality of electrically conductive members" in conjunction with "solder connections between said first plurality of electrically conductive members and said semiconductor chip", based on the same arguments as presented *supra* by Appellants in the first example relating to claim 80.

A second example of why Peterson does not teach each and every feature of claim 87, Peterson does not teach the following feature of claim 87: "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip", based on the same arguments as presented *supra* by Appellants in the second example relating to claim 80.

A third example of why Peterson does not teach each and every feature of claim 87, Peterson does not teach the following feature of claim 87: "providing a **semiconductor chip** having a first surface including a plurality of contact sites thereon" (emphasis added). The Examiner argues that Peterson discloses a semiconductor chip in col. 2, lines 2-3. In response, Appellant contends that col. 2, lines 1-3 of Peterson recite: "This cross-section also shows two device mounting pads (103 and 104) for soldering surface-mount devices." Appellants contend that the preceding teaching of Peterson does not explicitly disclose a semiconductor chip. Appellants further contend that the preceding teaching of Peterson does not inherently disclose a semiconductor chip, inasmuch as a surface-mount device may be a device other than a semiconductor chip.

Based on the preceding arguments, Appellants respectfully maintain that does not anticipate claim 87, and the claim 87 is in condition for allowance.

Claim 91

Appellants respectfully contend that Peterson et al. does not anticipate claim 91, because Peterson does not teach each and every feature of claim 91.

A first example of why Peterson does not teach each and every feature of claim 91, Peterson does not teach the following feature of claim 91: "each of said first and second pluralities of said electrically conductive members adapted for having solder connections **thereon** for being electrically connected to a semiconductor chip" (emphasis added), based on

the same arguments as presented *supra* by Appellants in the first example relating to claim 80.

A second example of why Peterson does not teach each and every feature of claim 91, Peterson does not teach the following feature of claim 91: "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip", based on the same arguments as presented *supra* by Appellants in the second example relating to claim 80.

A third example of why Peterson does not teach each and every feature of claim 91, Peterson does not teach the following feature of claim 91: "each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a **semiconductor chip**" (emphasis added). Appellants contend that Peterson does not teach a semiconductor chip and does not teach solder connections adapted to be connected to a semiconductor chip. In addition, since the Examiner has not addressed this feature of claim 91, Applicants contend that the Examiner has not satisfied the Examiner's burden of proof in relation to claim 91.

A fourth example of why Peterson does not teach each and every feature of claim 91, Peterson does not teach the following feature of claim 91: "positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprises a **first plurality of shielded**

signal conductors" (emphasis added). Appellants contend that Peterson does not disclose a first plurality of shielded signal conductors. In addition, since the Examiner has not addressed this feature of claim 91, Applicants contend that the Examiner has not satisfied the Examiner's burden of proof in relation to claim 91.

Claims 93-97

Since claims 93-97 depend from claim 91, which Appellants have argued *supra* to be patentable under 35 U.S.C. §102(b), Appellants maintain that claims 93-97 are patentable under 35 U.S.C. §102(b).

Issue 2

CLAIMS 81, 88, AND 92 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER PETERSON ET AL.

The Examiner rejected claims 81, 88, and 92 under 35 U.S.C. §103(a) as allegedly being unpatentable over Peterson et al.

Claim 81

Since claim 81 depends from claim 80, which Appellants have argued *supra* to be patentable under 35 U.S.C. §102(b), Appellants maintain that claim 81 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants contend that Peterson does not teach the following feature of

claim 81: "wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F".

The Examiner argues: "Regarding claims 81 and 92, Peterson et al. disclose the step of laminating except for the specific range of temperature and pressure. At the time the invention was made it would have been obvious matter of design choice to one having ordinary skill in the art to specify a specific range of temperature and pressure in the step of lamination because Applicant have not disclose that the specific temperature and pressure provide an advantage, are used for a particular purpose, or solve a stated problem. One ordinary skin in the art would have expected Applicants' invention to perform equally well as Peterson et al.'s invention. Therefore, it would have been obvious matter of design choice to specify a specific range of temperature and pressure in the step of laminating the first and second dielectric layers onto the thermally conductive layer to obtain the invention as specified in claims 81 and 92."

In response to the preceding argument by the Examiner, Appellants contend that the Examiner's argument is not persuasive, because the Examiner has not demonstrated that one of ordinary skill in the art would, as a matter of design choice, laminate at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F. Design choice is literally a "choice" and different designers would **choose** different ranges of pressure and temperature. The Examiner has not supplied any evidence that the designer would choose a pressure of from about 1000 to about 1500 psi and a temperature of from about 600 to about 750 ° F.

In order to establish a *prima facia* case of obviousness, the Examiner must supply an additional reference(s) evidencing performance of said laminating at a pressure and temperature in the ranges recited in claim 81, which the Examiner has not done. Accordingly, Appellants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 81.

Claim 88

Since claim 88 depends from claim 87, which Appellants have argued *supra* to be patentable under 35 U.S.C. §102(b), Appellants maintain that claim 88 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants contend that Peterson does not teach the following features of claim 88: "applying a first solder paste onto said conductive layer; and reflowing said solder paste to form a first plurality of solder connections."

The Examiner admits: "Regarding claim 88, Peterson et al. disclose forming a plurality of open in third dielectric layer (Fig. 1) that exposing a portion of the first plurality of electrically conductive members; plating a conductive layer to form a plurality of microvias (106, 107; etc.), but Peterson et al. do not disclose step of applying and re-flowing a first solder paste."

The Examiner argues: "It would have been obvious matter of design choice to one having ordinary skill in the art at the time the invention was made to apply and re-flow a first solder paste onto the conductive layer because Applicant have not disclose that the steps of applying and re-flowing a first solder paste onto the conductive layer provide an advantage, are used for a

particular purpose, or solve a stated problem. One ordinary skill in the art would have expected Applicants' invention to perform equally well with either without applying and re-flowing a first solder paste onto the conductive layer as taught by Peterson et al. or with claimed invention. Therefore, it would have been obvious matter of design choice to modify Peterson et al. to obtain the invention as specified in claim 88."

In response to the preceding argument by the Examiner, Appellants contend that the Examiner's argument is not persuasive, because the Examiner has not demonstrated that one of ordinary skill in the art would, as a matter of design choice, perform the steps of applying and reflowing the solder paste on the conductive layer to form a first plurality of solder connections" in accordance with the requirements of claim 88. In order to establish a *prima facia* case of obviousness, the Examiner must supply an additional reference(s) that performs said applying and reflowing steps, and provide a persuasive argument as to why it would be obvious to modify Peterson with said additional reference(s), which the Examiner has not done. Accordingly, Appellants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 88.

Claim 92

Since claim 92 depends from claim 91, which Appellants have argued *supra* to be patentable under 35 U.S.C. §102(b), Appellants maintain that claim 92 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants contend that Peterson does not teach the following feature of

claim 92: "wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F".

The Examiner argues: "Regarding claims 81 and 92, Peterson et al. disclose the step of laminating except for the specific range of temperature and pressure. At the time the invention was made it would have been obvious matter of design choice to one having ordinary skill in the art to specify a specific range of temperature and pressure in the step of lamination because Applicant have not disclose that the specific temperature and pressure provide an advantage, are used for a particular purpose, or solve a stated problem. One ordinary skin in the art would have expected Applicants' invention to perform equally well as Peterson et al.'s invention. Therefore, it would have been obvious matter of design choice to specify a specific range of temperature and pressure in the step of laminating the first and second dielectric layers onto the thermally conductive layer to obtain the invention as specified in claims 81 and 92."

In response to the preceding argument by the Examiner, Appellants contend that the Examiner's argument is not persuasive, because the Examiner has not demonstrated that one of ordinary skill in the art would, as a matter of design choice, laminate at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F. Design choice is literally a "choice" and different designers would **choose** different ranges of pressure and temperature. The Examiner has not supplied any evidence that the designer would choose a pressure of from about 1000 to about 1500 psi and a temperature of from about 600 to about 750 ° F.

In order to establish a *prima facia* case of obviousness, the Examiner must supply an additional reference(s) evidencing performance of said laminating at a pressure and temperature in the ranges recited in claim 92, which the Examiner has not done. Accordingly, Appellants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 92.

Issue 3

CLAIMS 89 AND 90 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER PETERSON ET AL. IN VIEW OF US PATENT 5,691,041 TO FRANKENY ET AL.

The Examiner rejected claims 89 and 90 under 35 U.S.C. §103(a) as allegedly being unpatentable over Peterson et al. in view of US Patent 5,691,041 to Frankeny et al.

Claim 89

Since claim 89 depends from claim 87, which Appellants have argued *supra* to be patentable under 35 U.S.C. §102(b), Appellants maintain that claim 89 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants contend that Peterson does not teach the following feature of claim 89: "applying a second solder paste onto said respective ones of said first plurality of solder connections, positioning said respective ones of said contact members of said semiconductor chip against said respective ones of said first plurality of solder connections, and reflowing said second solder paste and said respective ones of said first plurality of solder

connections to electrically connect said semiconductor chip to said multi-layered interconnect structure".

The Examiner admits: "Regarding claim 89, Peterson et al. disclose the claim invention except for applying a second solder paste on solder connection, positioning the contact member of semiconductor chip against solder connection, and reflowing second solder paste to electrically connect said semiconductor chip to the multi-layer interconnect structure."

The Examiner argues: "However, Frankeny et al. disclose those steps (Fig. 6 and Col. 1, lines 43-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to add the steps of applying a second solder paste on solder connection, positioning the contact member of semiconductor chip against solder connection, and reflowing second solder paste to Peterson et al.'s method for electrically connecting said semiconductor chip to the multi-layer interconnect structure as taught by Frankeny et al."

In response to the preceding argument by the Examiner, Appellants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 89, because the Examiner has not provided a persuasive reason for modifying Peterson with Frankeny. In fact, the Examiner has not provided any reason for modifying Peterson with Frankeny.

Claim 90

Since claim 90 depends from claim 87, which Appellants have argued *supra* to be patentable under 35 U.S.C. §102(b), Appellants maintain that claim 90 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants contend that Peterson does not teach the following feature of claim 90: "connecting respective ones of said second plurality of said solder connections to respective ones of said plurality of contact pads on said circuitized substrate to make electrical connections therebetween".

The Examiner admits: "Regarding claim 90, Peterson et al. disclose the step of proving a second plurality of solder connection (104) for connect to surface mounting device not to a circuitized substrate".

The Examiner argues: "Frankeny et al. shows a circuitized substrate (10) connecting with second plurality of solder connections (Fig. 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuitized substrate as taught by Frankeny et al for connecting Peterson et al.'s second plurality of solder connection to a Frankeny et al.'s circuit board, in order to obtain the claimed invention."

In response to the preceding argument by the Examiner, Appellants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 92., because the Examiner has not provided a persuasive reason for modifying Peterson with Frankeny. The Examiner's reason for modifying Peterson with Frankeny is "to obtain the claimed invention", which is not a persuasive reason since at the time at which the present patent application was filed, one of ordinary skill in the art was not aware of the claimed invention. Additionally, the Examiner's reason is not persuasive, because the Examiner has not provided a reason in the context of what effect the modification would have on the Peterson invention and why it would be obvious to modify Peterson with Frankeny for achieving such an effect.

Accordingly, Appellants contend that the Examiner has not established a *prima facie* case

of obviousness in relation to claim 90.

SUMMARY

In summary, Appellants respectfully request reversal in the office action of April 23, 2003 of: the rejection of claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b); and the rejection of claims 81, 88-90, and 92 under 35 U.S.C. §103(a)

Respectfully submitted,

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For: **ELECTRONIC PACKAGE FOR ELECTRONIC COMPONENTS AND METHOD OF MAKING SAME**

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APPENDIX - CLAIMS ON APPEAL

80. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections

between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

81. The method of making the multi-layered interconnect structure of claim 80 wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 °F.

82. The method of making the multi-layered interconnect structure of claim 80 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a first copper foil and a second copper foil respectively onto said first and second dielectric layers; and

etching selected portions of said first and second copper foils to respectively produce first and second pluralities of said electrically conductive members.

83. The method of making the multi-layered interconnect structure of claim 80 further including the steps of:

positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members;

removing portions of said third dielectric layer to expose portions of said first plurality

of electrically conductive members; and

forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

84. The method of making the multi-layered interconnect structure of claim 83 wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

85. The method of making the multi-layered interconnect structure of claim 80 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;

removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and

forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

86. The method of making the multi-layered interconnect structure of claim 85 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.

87. A method of making an electronic package comprising the steps of:

providing a semiconductor chip having a first surface including a plurality of contact sites thereon;

providing a multi-layered interconnect structure adapted for electrically interconnecting said semiconductor chip to a circuitized substrate, said multi-layered interconnect structure including a thermally conductive layer, having first and second opposing surfaces, first and second dielectric layers positioned on said first and second opposing surfaces, respectively, and first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively;

providing a first plurality of solder connections on said first plurality of electrically conductive members; and

connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact sites on said semiconductor chip, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip.

88. The method of making the electronic package of claim 87 further comprising positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members, wherein said step of providing said first plurality of solder connections on said first plurality of electrically conductive members includes:

forming a plurality of openings in said third dielectric layer, each of said openings

including an internal wall and exposing a portion of at least one of said first plurality of electrically conductive members;

plating a conductive layer on said internal wall of said plurality of openings and on

said exposed portion of said at least one of said first plurality of electrically conductive members to define a plurality of microvias;

applying a first solder paste onto said conductive layer; and

reflowing said solder paste to form a first plurality of solder connections.

89. The method of making the electronic package of claim 88 wherein said step of connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact members on said semiconductor chip further includes the steps of applying a second solder paste onto said respective ones of said first plurality of solder connections, positioning said respective ones of said contact members of said semiconductor chip against said respective ones of said first plurality of solder connections, and reflowing said second solder paste and said respective ones of said first plurality of solder connections to electrically connect said semiconductor chip to said multi-layered interconnect structure.

90. The method of making the electronic package of claim 87 further including the steps of:

providing a circuitized substrate having a first surface including a plurality of contact pads thereon;

providing a second plurality of solder connections on said second plurality of conductive members of said multi-layered interconnect structure; and

connecting respective ones of said second plurality of said solder connections to respective ones of said plurality of contact pads on said circuitized substrate to make electrical connections therebetween.

91. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively;

positioning a first electrically conductive layer within said first dielectric layer;

positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

92. The method of making the multi-layered interconnect structure of claim 91 wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second

dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F.

93. The method of making the multi-layered interconnect structure of claim 91 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a copper foil onto said first and second dielectric layers; and

etching selected portions of said copper foil to produce first and second pluralities of said electrically conductive members.

94. The method of making the multi-layered interconnect structure of claim 91 further including the steps of:

positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members;

removing portions of said third dielectric layer to expose portions of said first plurality of electrically conductive members; and

forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

95. The method of making the multi-layered interconnect structure of claim 94 wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

96. The method of making the multi-layered interconnect structure of claim 91 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;

removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and

forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

97. The method of making the multi-layered interconnect structure of claim 96 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.